



Berenbaum 9-4-5-5

#13
1 of 3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

5 Applicant(s): Berenbaum et al.
Case: 9-4-5-5
Serial No.: 09/538,755
Filing Date: March 30, 2000
Group: 2154
10 Examiner: Larry D. Donaghue

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450

Signature: [Signature] Date: May 25, 2004

Title: Method and Apparatus for Splitting Packets in a Multithreaded VLIW Processor

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REPLY BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

Appellants hereby reply to the Examiner's Answer, mailed March 31, 2004, in an Appeal of the final rejection of claims 1 through 16 in the above-identified
25 patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal Brief.

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RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief.

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STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief.

SUMMARY OF INVENTION

A Summary of the Invention is contained in Appellants' Appeal Brief.

ISSUES PRESENTED FOR REVIEW

A statement identifying the issues present for review is contained in Appellants' Appeal Brief.

GROUPING OF CLAIMS

The rejected claims stand and fall together.

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

ARGUMENT

In the Examiner's answer, the Examiner asserts that it is not claimed or disclosed in the present application that the allocation of instructions is done independently of the type of instruction ready for execution within each thread. The Examiner further asserts that the phrase, "the illustrative Multithreaded VLIW processor 600 includes nine functional units 620-1 through 620-9, which can be allocated independently to any thread TA-TC," means that the "functional units are not all assign to one packet, but can be split across multi-packet and each packet representing a different thread."

As the Examiner notes, the functional units are not all assigned to one packet; the functional units can be allocated to any thread. Appellants note, however, that in order to *independently* allocate functional units to threads, the allocation *must* be independent of the instruction type. If this were not the case, the allocation would

depend on the instruction type and, therefore, the allocation of a functional unit to a thread would *depend* upon the type of instruction ready for execution in said thread. Stated another way, a thread would determine which functional units could be allocated to it. Thus, the allocation of the functional units would be *dependent on, and not*
5 *independent of*, the threads.

Conclusion

The rejections of the independent claims under section §102 in view of Chung et al. and Keckler et al., alone or in any combination, are therefore believed to be
10 improper and should be withdrawn. The rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,



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Date: May 25, 2004